



# Optimization of sputtered Cr/Au thin film for diaphragm-based MEMS applications

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## ABSTRACT

An optimization study on the sputtering of Cr/Au thin film for diaphragm-based MEMS applications is presented. The effects of the film thickness, process pressure and process power on the residual stress of the film are investigated. A low-stress silicon nitride diaphragm-based device characterization platform is fabricated to study the influence of the Cr/Au film stress on the diaphragm compliance. The fabricated devices are characterized by measuring the capacitance change under a bias voltage from 0 to 40 V. For the 8- $\mu\text{m}$  and 10- $\mu\text{m}$  air gap device characterization platforms, the largest capacitance changes of 5.1% and 4.3%, respectively, occur at a compressive film stress of  $-200$  MPa. A large capacitance change indicates a more sensitive diaphragm, which is desired in pressure sensor design.

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## 1. Introduction

Residual stresses in thin films always present a major challenge during the design and fabrication of microelectromechanical system (MEMS) devices. Almost all thin film deposition techniques will result in residual stresses in the deposited films. Residual stresses in thin films originate from the reaggregation of the crystalline grains of the film materials during the deposition process. For multi-layered thin film structure, the origin of the residual stress lies in the difference in the coefficients of thermal expansion between the different materials.

Thin film sputtering has many advantages such as a wide choice of target materials, better step coverage, good uniformity over large area, small shadow effect and good adhesion. One important feature of sputtering is its many parameters that can be controlled to influence the film characteristics, which include the residual stress, film density and adhesion strength. Typical control parameters include the process pressure, substrate temperature, process power and substrate bias voltage. By varying the process pressure, the film stress can be altered. The transition region between the compressive and tensile stress is often very sudden and sharp, which can lead to unpredictable results. For low-stress diaphragm-based applications, the narrow stress transition window makes the crossover point (ideal for zero-stress film) very difficult to control.

Evaporation of metallic thin film as an electrode layer in diaphragm-based acoustic MEMS devices has been well-documented [1–4]. The advantages of evaporation are low residual stress and good quality of the deposited film as compared to sputtering. However, for the evaporation process, it is difficult to control the film properties, such as film thickness, grain size and step coverage, and thus, it is not as

controllable as the sputtering process [5]. In addition, there are limited data on the effect of the evaporation parameters on the residual stress of the deposited film. However, a handful of sputtering parameters can be investigated for their influences on the film stress [6–10].

In this work, the effects of the type of film materials, film thickness, process pressure and process power on the residual stress are studied. Next, using these experimental data obtained, further investigation is carried out to examine the effect of the electrode film stress on the mechanical compliance of a silicon nitride ( $\text{Si}_3\text{N}_4$ ) diaphragm-based device characterization platform. The fabrication process and the electrical characterization results of the device platform are also furnished in details.

## 2. Material selection

Table 1 tabulates the coefficient of thermal expansion (CTE) of several materials at room temperature. As mentioned earlier, the difference in CTE values between the materials is mainly responsible for the residual stress induced in the multi-layered film structure. The larger the difference in CTE values between the materials, the higher is the induced stress in the deposited film. For an aluminium (Al) metallization scheme on a low pressure chemical vapour deposition (LPCVD)  $\text{Si}_3\text{N}_4$  diaphragm [1–3], a large disparity (i.e. large film stress) in CTE values ( $21.5 \times 10^{-6}/^\circ\text{C}$ ) exists between the materials. This large difference in CTE value can be minimised to  $12.6 \times 10^{-6}/^\circ\text{C}$  by utilizing the gold (Au) metallization scheme [2]. However, there is a potential adhesion reliability issue here as Au requires an adhesion layer between itself and the substrate surface. Chromium (Cr) [4] and titanium (Ti) [3] are two commonly used adhesion layer materials for Au film deposition. However, Cr is a better choice than Ti in the diaphragm applications as its CTE ( $4.9 \times 10^{-6}/^\circ\text{C}$ ) is closer to that of LPCVD  $\text{Si}_3\text{N}_4$  film ( $1.6 \times 10^{-6}/^\circ\text{C}$ ) than that of Ti ( $8.6 \times 10^{-6}/^\circ\text{C}$ ). Therefore, this dual-layered Cr/Au metallization scheme offers good

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**Table 1**  
Tabulation of coefficient of thermal expansion of selected materials.

Materials	Value ( $10^{-6}/^{\circ}\text{C}$ at $25^{\circ}\text{C}$ )
Aluminum (Al) <sup>a</sup>	23.1
Gold (Au) <sup>a</sup>	14.2
Titanium (Ti) <sup>a</sup>	8.6
Chromium (Cr) <sup>a</sup>	4.9
Silicon (Si) <sup>a</sup>	2.6
LPCVD silicon nitride ( $\text{Si}_3\text{N}_4$ ) <sup>b</sup>	1.6

<sup>a</sup> [11].

<sup>b</sup> [5].

adhesion property and potentially lower residual stress since a multi-layered thin film structure tends to have a lower overall residual stress [12]. As a result, a Cr/Au metallization scheme is selected for further investigation work.

### 3. Experimental details

In this experimental study, the film thickness, process pressure and process power are investigated for their influences on the residual stress of the sputtered Cr/Au thin film. The DC/RF Magnetron sputtering system in the laboratory has been previously optimized for metal sputtering at 3 mTorr process pressure, 200 W process power and 0 V substrate bias voltage in room temperature environment. The sputtering chamber is pumped down to about 1.5 to 1.8  $\mu\text{Torr}$  prior to the commencement of any sputtering processes. A thin layer of Cr/Au film is sputtered onto a 4-inch  $\langle 100 \rangle$ -orientated silicon wafer and the resulting film stress is characterized by Tencor FLX-2908 laser profilometry-based stress measurement equipment using Stoney's Equation [13], which can be expressed by

$$\sigma = \frac{E}{1-\nu} \cdot \frac{1}{6} \cdot \frac{t_s^2}{t_f} \cdot \frac{1}{R} \quad (1)$$

$$R = \frac{R_1 R_2}{R_1 - R_2} \quad (2)$$

where  $E$  is the elastic modulus of (100) silicon wafer ( $1.3 \times 10^{11}$  Pa),  $\nu$  is the Poisson's ratio of (100) silicon wafer (0.28),  $t_s$  is the substrate thickness,  $t_f$  is the film thickness,  $R_1$  is the wafer curvature before sputtering and  $R_2$  is the wafer curvature after sputtering.

## 4. Results and discussions

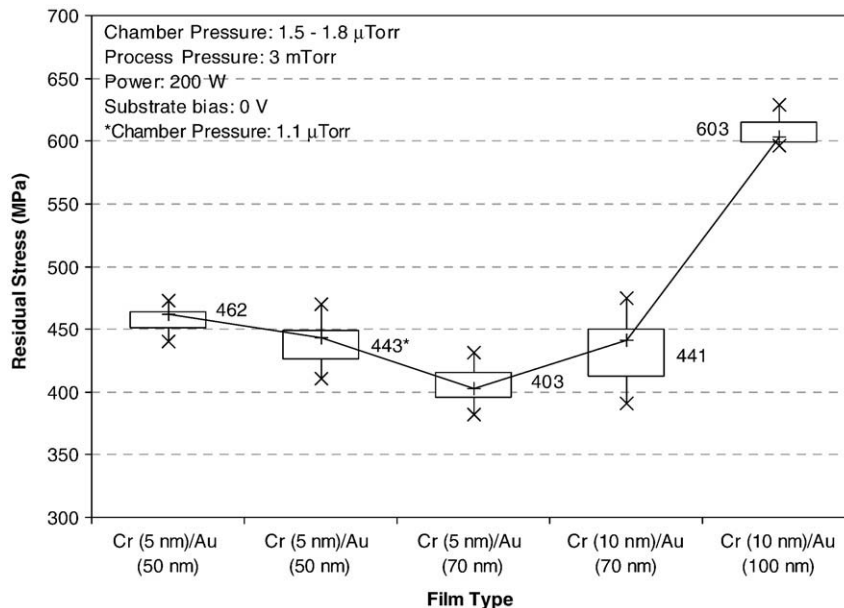
### 4.1. Film thickness

Generally, a thicker deposited film tends to result in a higher induced residual stress. Fig. 1 illustrates the effect of the film thickness on the residual stress of the sputtered Cr/Au film. As illustrated in Fig. 1, the largest stress reduction occurs when the Au thickness is reduced from 100 nm (603 MPa) to 70 nm (441 MPa) when the Cr thickness is at 10 nm. When the Cr thickness is decreased to 5 nm with the Au thickness at 70 nm, the film stress further reduces to 403 MPa. However, when the Au thickness is further lowered to 50 nm with the Cr thickness at 5 nm, no further stress reduction can be observed. On the contrary, an increase in stress (462 MPa) is recorded. A repeated Cr (5 nm)/Au (50 nm) sputtering experiment at 1.1  $\mu\text{Torr}$  chamber pressure yields almost similar stress result (443 MPa).

Inside the sputtering chamber, a total of four 4-inch wafers can be loaded on a revolving substrate holder plate while the four target materials are stationary. It takes about 15 s to complete a full revolution of the substrate holder plate. However, for a 5 nm thick Cr film, the sputtering process requires about 20 s. As a result, there is a potential adhesion reliability issue here as all four wafers may not be evenly sputtered to the desired thickness. Fig. 1 also highlights that when the thicknesses of the Cr and Au layers are at or below 10 nm and 70 nm, respectively, the maximum stress deviation is only 59 MPa. Thus, to avoid adhesion reliability issue in future, a 10 nm thick Cr adhesion layer is preferred and the price to pay for it is only an increase of 38 MPa in residual stress. Hence, the metallization scheme of Cr (10 nm)/Au (70 nm) represents an optimized compromise between low residual stress and good adhesion reliability.

### 4.2. Process pressure

Fig. 2 illustrates the effect of the process pressure on the residual stress of the sputtered Cr/Au film. As illustrated in Fig. 2, there is a narrow stress transition window, which occurs between 5.8 mTorr (280 MPa) and 6.0 mTorr ( $-189$  MPa), and this represents a very large stress gradient of  $-2345$  MPa/mTorr, which is significantly higher than the stress gradients before and after the transition window. From a process pressure of 1.0 to 5.8 mTorr, the film stress is tensile and shows a gradual decrease from 520 to 280 MPa. Beyond the



**Fig. 1.** Effect of the film thickness on the residual stress of the sputtered Cr/Au film.

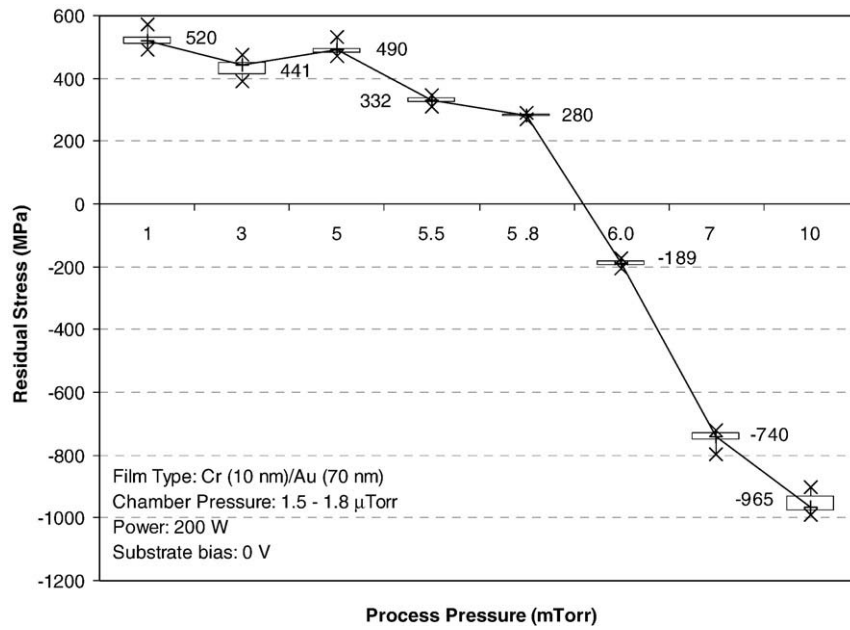


Fig. 2. Effect of the process pressure on the residual stress of the sputtered Cr/Au film.

transition window from 6.0 to 10.0 mTorr, the stress is compressive and shows an increase from  $-189$  to  $-965$  MPa. Hence, when the process pressure is increased, the film stress reduces and transits from tension to compression with a sudden sharp drop between 5.8 and 6.0 mTorr.

#### 4.3. Process power

Fig. 3 illustrates the effect of the process power on the residual stress of the sputtered Cr/Au film. As illustrated in Fig. 3, when the process power is varied from 175 to 200 W, the film stress shows a gradual decrease in compressive stress until it reaches its minimum value ( $-189$  MPa) at 200 W. After that, the stress increases to  $-325$  MPa at 210 W. Since the stress fluctuation is about 145 MPa from 175 to 210 W, the effect of the process power on the film stress is not as dominant as that of the process pressure.

#### 4.4. Fabrication of the device characterization platform

Fig. 4 illustrates the two-wafer fabrication sequence of the device characterization platform. For the diaphragm wafer, a layer of low-stress (about 20 to 34 MPa) LPCVD  $\text{Si}_3\text{N}_4$  ( $0.5 \mu\text{m}$  thickness) is deposited and patterned on one side of the  $\langle 100 \rangle$ -orientated silicon wafer (Fig. 4a). The patterned  $\text{Si}_3\text{N}_4$  layer will subsequently function as a mask during the release of the  $\text{Si}_3\text{N}_4$  diaphragm ( $4 \times 4$  mm) on the opposite side during the KOH wet etching process at  $80^\circ\text{C}$  (Fig. 4b). After that, a layer of Cr (10 nm)/Au (70 nm) is sputtered onto the diaphragm as an electrode layer (Fig. 4c). Finally, the diaphragm wafer is diced to release the individual diaphragm dies.

For the backplate wafer (low wafer resistivity of 0.001 to  $0.01 \Omega \text{ cm}$ ), a layer of photoresist and bonding polymer is spin-coated and patterned on the top side of the wafer (Fig. 4d). Next, the reactive ion etch (RIE) step is performed to form an air gap cavity (cavities of 8 and

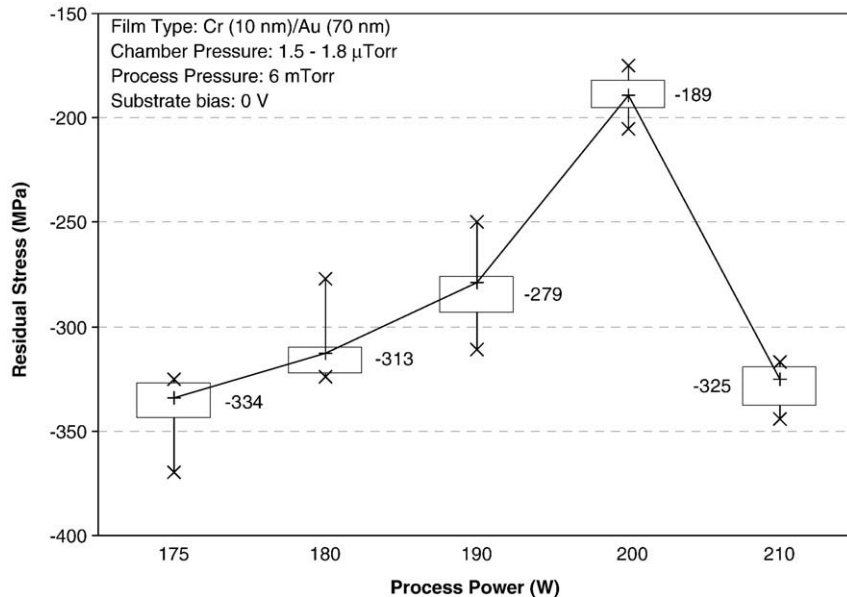
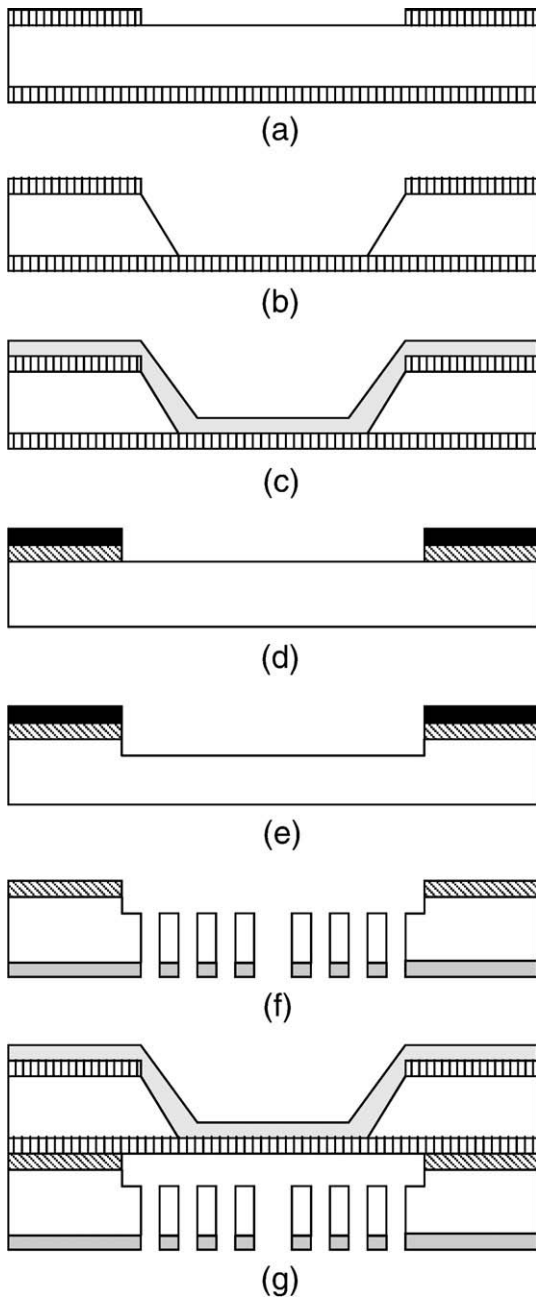


Fig. 3. Effect of the process power on the residual stress of the sputtered Cr/Au film.



**Fig. 4.** Fabrication sequence of the device characterization platform: (a) LPCVD and patterning of  $\text{Si}_3\text{N}_4$  layer, (b) KOH etching to release diaphragm, (c) sputtering of Cr/Au to form electrode, (d) spin-coating and patterning of photoresist (top layer) and bonding polymer (bottom layer), (e) RIE etching to form a 8/10- $\mu\text{m}$  deep air cavity, (f) deep RIE etching to form slots and holes and sputtering of Ti/Au to form electrode, and (g) thermal polymer bonding of diaphragm and backplate dies.

10  $\mu\text{m}$  are etched) in the wafer (Fig. 4e). Then, the bottom side of the wafer is patterned and deeply etched to form the slots (0.6 mm wide) and holes (80  $\mu\text{m}$  diameter) (Fig. 4f). The size of the backplate excluding the slots is 2.8  $\times$  2.8 mm. Slots [14] and holes [1–4] in the backplate are required to provide some amount of mechanical damping for the diaphragm. During the deep etching process, the individual backplate dies are also released from the backplate wafer. After that, a layer of Ti (10 nm)/Au (200 nm) is sputtered onto the backplate dies to form the electrode layer. Finally, the diaphragm and the backplate dies are bonded together thermally at a temperature of 160  $^\circ\text{C}$  (Fig. 4g). Fig. 5 shows the top diaphragm view (left) and bottom backplate view (right) of an assembled device characterization platform.

#### 4.5. Electrical characterization

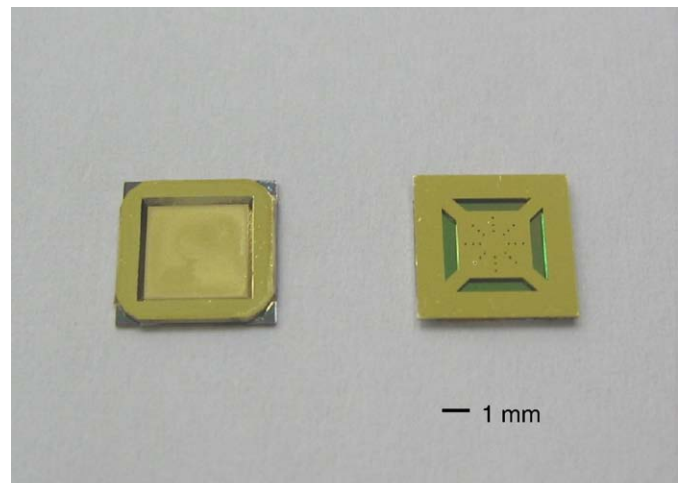
For the electrical characterization of the assembled device characterization platform, a Hewlett-Packard 4284A Precision LCR meter is used to measure the capacitance change when a bias voltage from 0 to 40 V is applied to the electrodes. The residual stress value in Figs. 6 and 7 is referenced to a silicon wafer, which is also placed in the sputtering chamber alongside the diaphragm wafer during the sputtering process. After sputtering, the silicon wafer is taken out of the chamber for stress characterization.

Fig. 6 illustrates the capacitance-voltage (C-V) curves for the 10- $\mu\text{m}$  air gap device characterization platform. As illustrated in Fig. 6, the C-V curves for both 603 MPa and 718 MPa residual stresses are similar. At a tensile stress of 603 MPa, the capacitance change is only 0.4% at a bias voltage of 40 V. At 441 MPa (a stress reduction of 26.9%) and 405 MPa (a stress reduction of 32.8%), the capacitance changes increase to 1.6% and 2.3%, respectively. However, the largest capacitance change of 4.3% is observed at a compressive stress of  $-200$  MPa. This represents a capacitance change of nearly 11 times higher as compared to a tensile stress of 603 MPa. A large capacitance change indicates a more sensitive diaphragm.

Fig. 7 illustrates the C-V curves for the 8- $\mu\text{m}$  air gap device characterization platform. As illustrated in Fig. 7, the smallest capacitance change of 0.8% is observed at a residual stress of 603 MPa. At 441 MPa and 405 MPa, the capacitance changes enhance to 2.5% and 3.3%, respectively. Similarly, the largest capacitance change of 5.1% is observed at a compressive stress of  $-200$  MPa when the bias voltage is 38 V.

#### 5. Conclusion

The sputtering parameters of the film thickness, process pressure and process power are investigated. Using the experimental results obtained, a Cr/Au electrode layer is sputtered onto a low-stress  $\text{Si}_3\text{N}_4$  diaphragm-based device characterization platform to examine the effect of the residual stress on the compliance of the diaphragm. For the metallization scheme, a layer of Cr (10 nm)/Au (70 nm) represents a good compromise between low stress level and good adhesion reliability. For the process pressure, the narrow stress transition window occurs between 5.8 mTorr (280 MPa) and 6.0 mTorr ( $-189$  MPa). For the process power, its effect on the residual stress is not as dominant as that of the process pressure. For the 10- $\mu\text{m}$  air gap device characterization platform, the largest capacitance change (4.3%) occurs at a compressive stress of  $-200$  MPa. For the 8- $\mu\text{m}$  air gap device characterization platform, the largest capacitance change (5.1%) occurs



**Fig. 5.** A photograph of an assembled device characterization platform.

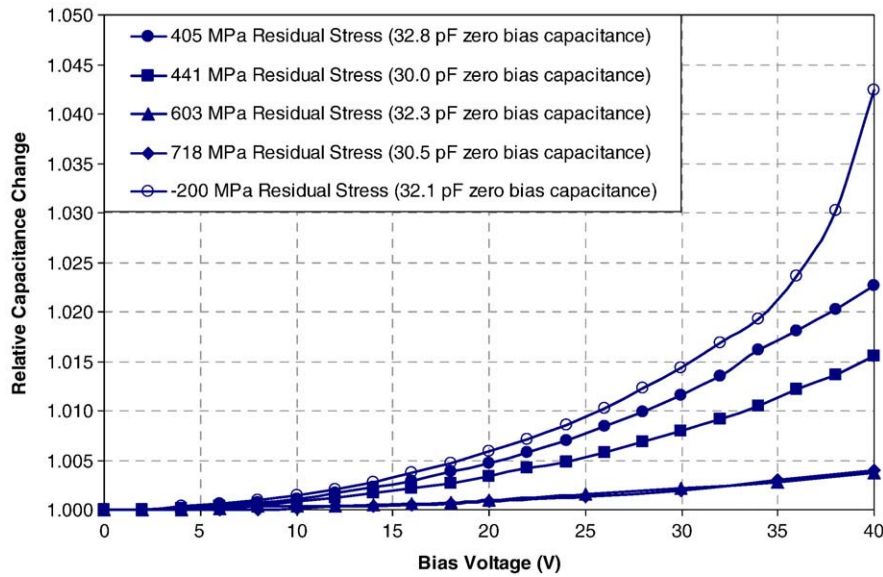


Fig. 6. Capacitance-voltage (C-V) curves for the 10- $\mu\text{m}$  air gap device characterization platform.

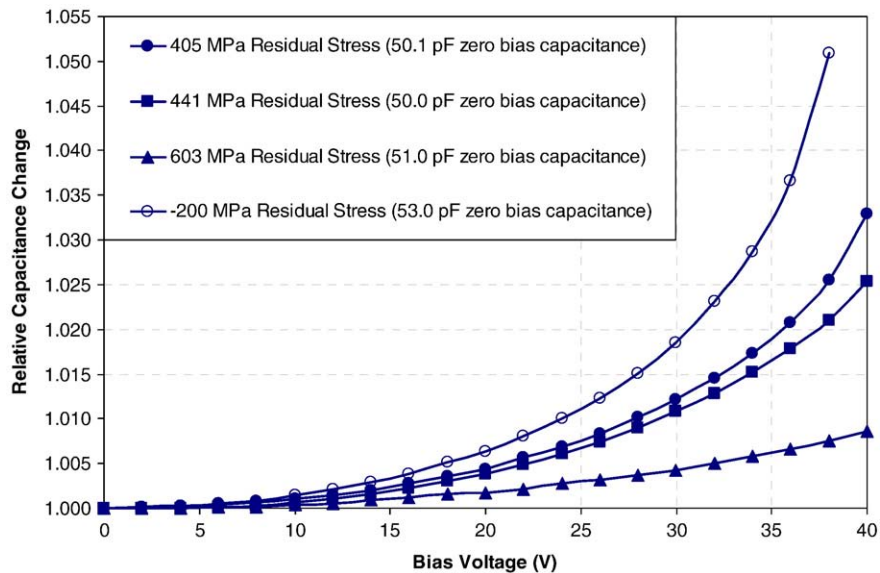


Fig. 7. Capacitance-voltage (C-V) curves for the 8- $\mu\text{m}$  air gap device characterization platform.

at  $-200$  MPa. A large capacitance change indicates a more sensitive diaphragm, which is desired in pressure sensing applications.

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